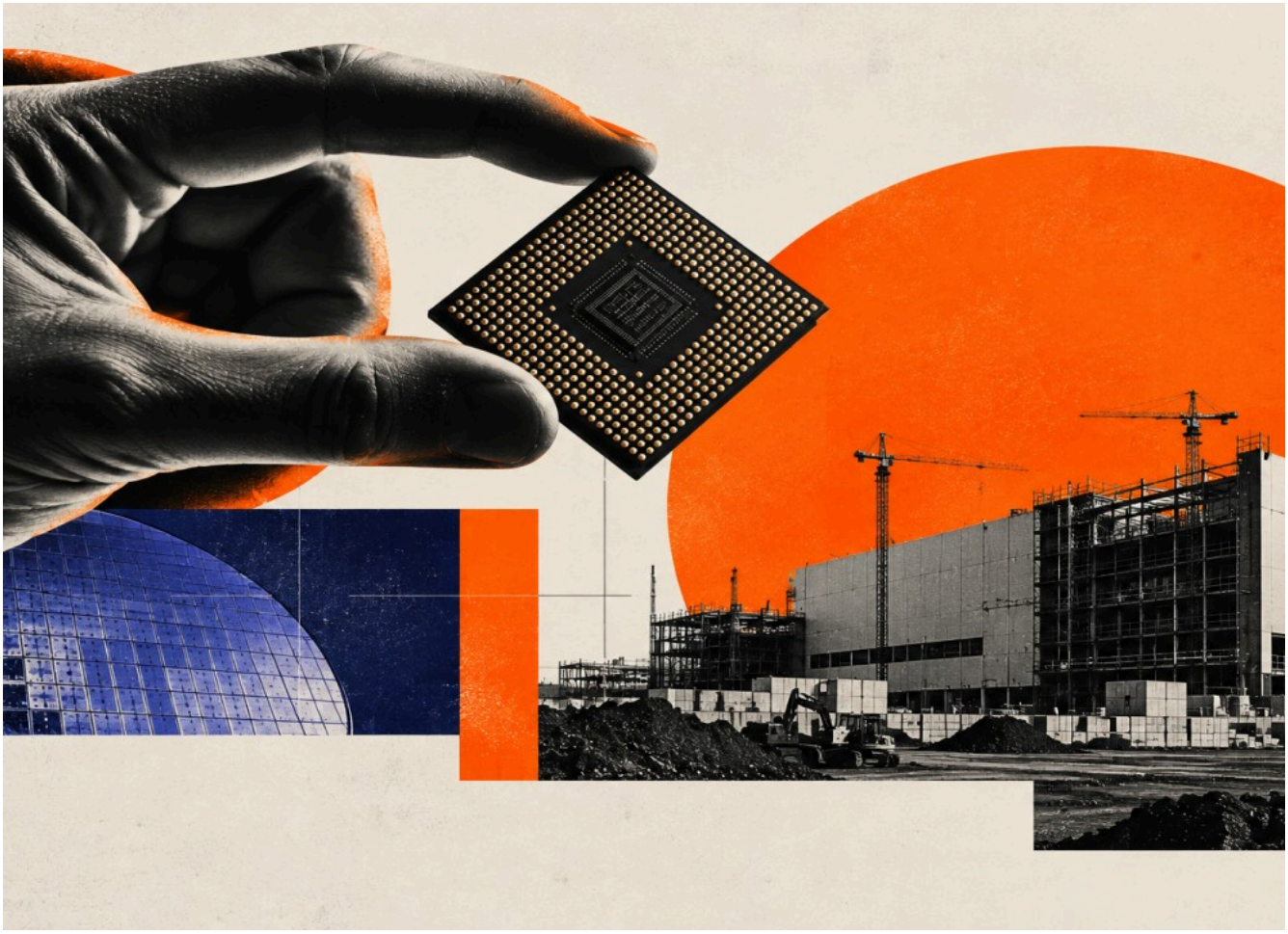
India’s semiconductor ambition is all packaging, no chips

Government subsidies have drawn companies into basic chip packaging, where China and Malaysia already hold an edge. Moving up the value chain may prove to be a stiff task.



There is just one genuine chip fabrication plant on the list. Tata’s Rs 91,526 crore fab, being built with Taiwan’s PSMC in Dholera, Gujarat, remains under construction and is not expected to produce chips commercially before 2028. Until then, India’s semiconductor ambitions will rest largely on packaging.

Even that may not be enough to build a competitive industry. Much of the planned capacity involves older packaging technologies, where China and Malaysia have spent years building scale, expertise and supply chains. Indian companies will have to compete against established players in a market where cost advantages are hard to come by. A single Chinese company, for instance, packages more chips in a year than India’s entire build-out thus far is designed to handle. And Malaysia, which has been in the business for five decades, is also investing RM25 billion (Rs 58,000 crore or $6 billion) to move beyond packaging into higher-value parts of the semiconductor supply chain.

India, thus, is entering an industry at a level that its competitors are already looking to move beyond. The reason for this lies in how the government designed its incentives in the first place, encouraging companies to take the easiest route into the semiconductor business, rather than build capabilities that could give the country a meaningful place in the global supply chain.

A low bar

Chip-making has two broad stages. First, a fab prints circuits onto silicon wafers, a hugely technical process. Then comes packaging, which involves assembling, connecting and sealing chips before they are shipped to customers. It is a far easier business to enter.

When India launched its semiconductor scheme in December 2021, the government appeared to recognize this distinction. Packaging projects were eligible for 30% of their cost, against 50% for actual fabs. But with few takers,the government revised the scheme nine months later. From September 2022, packaging projects became eligible for a flat 50% support, on par with fabs, regardless of the technology involved.

States piled on their own subsidies. Kaynes, for instance, receives 50% from the Centre and another 20% from Gujarat, covering roughly 70% of its eligible capital cost.

The flat rate is at the heart of the problem. It gives companies little incentive to invest in more advanced technologies. “No direct subsidy advantage existed. Conventional and advanced proposals received the same 50% headline central support,” says a senior government official. He spoke to The Morning Context on condition of anonymity**.**

Companies had to submit plans for upgrading their technology, but the central rules did not require them to follow through unless the conditions were written into their individual agreements. That meant a company could build the simplest wire-bond line and receive the same subsidy as one attempting the most advanced form of packaging. It is hardly surprising which route most companies took.

Take Kaynes Semicon. Approved in September 2024, it shipped its first packaged chip 13 months later: a power module for US customer Alpha & Omega Semiconductor. It uses wire bonding. As do CG Semi, a joint venture between CG Power, Japan’s Renesas and Thailand’s Stars Microelectronics, and Suchi Semicon’s Surat unit.

ISM 2.0, notified on 31 August, finally differentiates between technologies. Advanced packaging now qualifies for 35% support, while conventional packaging gets 25%. Both categories also require at least Rs 1,000 crore in investment and Rs 200 crore in existing revenue, which can include a parent group or joint venture.

The lower subsidy for conventional packaging, according to the senior government official, should be read “as a policy shift toward technology differentiation, not as an official admission that ISM 1.0 made an error”.

The change, however, comes too late for projects already approved under the earlier scheme. Those plants retain the terms of the original agreements.

The actual disbursement of subsidies has also lagged behind the commitments. Payments are made only when projects meet specified milestones. As a result, the scheme spent just 23% of its budget in 2023-24 and 9% in 2024-25. Spending picked up in 2025-26, reaching about 61% of the allocation. Overall, roughly Rs 5,600 crore was disbursed over the three years, according to budget data compiled by PRS Legislative Research. But the eventual bill could be higher. Based on the approved investments of Rs 68,000 crore across the projects, packaging-related subsidies could run as high as Rs 34,000 crore.

For all that spending, India would not be capturing much of what packaging generates. The operating plants import nearly everything they need. Suchi Semicon told The Morning Context that all its raw materials come from overseas. What is local is the assembly, testing and labour.

That raises a more basic question: how much is packaging worth?

Poor margins

People across the industry pointed to the relatively lower skill requirements and low labour costs as reasons why OSAT is a cheaper way to enter the semiconductor business.

But Sujata Seshadrinathan, co-founder and director of digital transformation at Basiz Fund Services, says that is only half the story. “OSAT is less risky than cutting-edge wafer fabrication, but it is certainly not a low-risk manufacturing business,” she says. Plants still need specialist engineers, customers can take years to win, and the costs don’t stop even when orders do.

The bigger problem is what Indian plants are packaging, and how. There are broadly three ways to package a chip. The oldest is wire bonding, in which a machine connects gold or copper wires from a chip to its casing, a lot like sewing on buttons. It is cheap and reliable, and is used in simpler chips found in cars, chargers and factory equipment, among other things.

Next is flip-chip, where the chip is turned face-down and pressed onto tiny solder bumps. Think of it as a stamp rather than a stitch: it allows more connections and faster signals. Then there is 2.5D packaging, where several chips sit side by side on a shared base. That is how many AI processors are built, and it is where the industry is moving towards.

Nearly every Indian plant currently packaging chips uses wire bonding or, at best, flip-chip. Only a handful of approved projects, such as 3D Glass Solutions’ Rs 1,944 crore plant in Odisha, target the advanced packaging technologies that the new scheme seeks to encourage.

Suchi Semicon illustrates the gap. Its Surat plant uses wire bonding, the company told The Morning Context. It plans to move to flip-chip and more advanced methods once its existing line settles down, with the next upgrade planned for early 2028.

This does not, in any way, mean that wire bonding is obsolete. It remains important to industries such as electric vehicles, power grids and industrial automation. Seshadrinathan argues that India is “not just building for yesterday”.

But high volumes do not necessarily translate to high value. Older-generation chips accounted for 88% of chips sold worldwide in 2023, but only 40% of sales by value. Amkor, one of the world’s largest packagers, now earns 83% of its revenue from advanced products. PwC expects the advanced packaging market alone to grow from $42 billion in 2024 to $76 billion by 2030.

Then again, China plays the conventional packaging game at a scale India can barely fathom. Four Chinese companies featured in market intelligence and research firm TrendForce’s latest global top-ten list of packagers in 2024. The largest, JCET, packaged 39.3 billion chips using traditional methods alone. India’s first lot of plants, by comparison, are designed to handle just over 24 billion chips a year.

Even at that scale, the margins are thin. JCET and Amkor, two of the world’s largest packagers, retained only about 14% of sales after direct costs. That leaves little room for Indian plants to absorb a cost disadvantage that the NITI Aayog estimates at 10-14% against China, with much of the materials they consume—from substrates to bonding wire—being imported.

Asked whether an Indian conventional packaging plant could compete on price with China or Malaysia, the senior government official quoted above said, “Not initially on unit cost alone.”

Suchi Semicon, which had earlier said it was price-competitive with South East Asia, offered a similar qualification to The Morning Context. “China’s pricing is difficult to match, given the significant government subsidies and its well-established local value chain.” Its competitiveness with South East Asia, the company said, is “supported by the benefits available through central and state government policies”, some of which it passes on to customers.

In other words, the advantage comes from subsidies, not an established cost edge of its own. Suchi expects “at least five years for the domestic ecosystem and local supply chain to stabilize and mature”.

The early numbers offer little reassurance. CG Power’s semiconductor business, which includes its Sanand packaging plant, reported an operating loss of about Rs 108 crore in FY26. Kaynes Technology’s packaging business is expected to start generating revenue only in the second half of this year.

Malaysia offers a cautionary example of what India could be getting into. It has been assembling chips since the 1970s and now handles about 13% of the world's assembly, testing and packaging.

Yet a 2026 study by Singapore's ISEAS-Yusof Ishak Institute found that the country’s semiconductor sector barely added more value than manufacturing as a whole: 22.3% in 2022, against 22.5% for manufacturing overall. Between 2012 and 2020, Malaysia-based firms filed 34 US semiconductor patents of their own. Korean firms filed 23,843.

The study points to a fundamental reason: assembly and packaging account for just 6% of the semiconductor industry's total value. Chip design and integrated chipmakers account for 57%.

That’s why Malaysia is now committing RM25 billion to move into chip design, advanced packaging and fabs. Industry players there, the study notes, already see India as a future rival in the very segment Malaysia is trying to move beyond. The official called this “a competitive warning”.

There’s another risk that India faces. If a plant simply cannot compete, the taxpayer carries the cost. The government can claw back incentives if a company commits fraud, goes bust, abandons the project and breaks its terms. Or, if it doesn’t stay the course for at least three years. But if the company fulfils all its obligations and then fails to be competitive in a global market, the public money is lost.

“Commercial difficulty alone is not the same as breach of an incentive agreement,” says the official. If a plant is built honestly, operates for the required three years and then struggles, the subsidy stays spent. Kaynes alone received Rs 170 crore in subsidy by July 2026.

Any way up the value chain?

There is, however, a case for starting where India has. ASE, now the world’s largest chip packager, began with basic assembly work in Taiwan in 1984. In fact, every packaging hub started out with the basics. Demand for wire bonding is booming, too. Kulicke & Soffa, the largest maker of wire-bonding machines, reported a 123% year-on-year jump in revenue in its latest quarter.

But the road ahead is long. Seshadrinathan estimates it will take three to five years for India to develop credible flip-chip capabilities and five to eight years to achieve competitive 2.5D packaging at scale, “that too assuming successful technology partnerships and customer qualification happen”.